REMARKS

Claims 22, 33, and 41 have been amended. Claims 23, 34, 45 have been canceled. Claims 1-17, 19-22, 24-33, 35-41, 43-44, 46-49, and 51 are pending.

Applicant's representative is grateful for the allowance of claims 7-10, 14-17, 19-21, 28-31, and 36-39.

Claims 1-6, 11-13, 22-27, and 33-35 stand rejected under 35 U.S.C. § 102(a) as being anticipated by CPP (Cambridge Parallel Processing Gamma II Plus Technical Overview). This rejection is respectfully traversed.

Claims 1 and 22 recite, *inter alia,* "a circuit coupled between said main memory and said plurality of processing elements, wherein said circuit is adapted for: writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements." Claim 11 and 33 recite, *inter alia,* " a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements ... wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time."

CPP is a technical overview of the architecture, programming languages, and support software of the Gamma II Plus series of computers. CPP, page iii. Referring to Fig. 2.1, it can be seen that the Gamma II Plus series of computers utilize an array memory as its primary storage unit. The architecture of the Gamma II Plus computer is clearly shown in Fig. 2.1. Significantly, the figure illustrates that the Master Control Unit ("MCU") is coupled in parallel with each one of the PEs which form the processor array and each processor of the processor array is directly coupled via respective 1-bit

connections to its own portion of the array memory. See page 2-10 ("Each PE has a one-bit wide, direct connection to its own section of the array memory" (emphasis supplied)).

The Office Action alleges that the MCU meets the data path circuit limitation in the above quoted language from independent claims 1, 11, 22, and 33. Reconsideration is requested. As noted on page 2-11, the MCU "... is mainly concerned with issuing instruction streams to the" PE array. The Office Action alleges that the MCU meets the data path circuit limitation by interpreting Fig. 2.6, which shows a more detailed diagram of the MCU, to construe the array interface as coupling the MCU to the PEs and the Array Support (ASU) to the memory array. This interpretation is in error, since it is inconsistent with Fig. 2.1 which fails to show the MCU as a data path circuit between the PE array and the array memory.

Additionally, CPP describes the Array Interface as: "The array address and the decoded instructions for the1-bit and 8-bit processors are buffered and distributed by array interface logic. The equivalent function for the array data is implemented by the ASU." CPP, page 2-13. It appears the Office Action interprets "array data" as data stored in the array memory, and offers the Array Support Unit as an interface between the MCU and the array memory. However, CPP describes the Array Support Unit as:

> The Array Support Unit (ASU) acts as an interface between the data bus within the MCU, ..., and the data bus in the array, whose width matches the edge size of the array.... When sending data to the array, the MCU data may either be replicated or zero extended (if necessary) to fill the array bus. When receiving data from the array, the MCU may (if necessary) select one of the words from the array data bus.
>
> CPP, page 2-12

The above quoted description does not require, as alleged by the Office Action, the ASU to interface with the array memory, since the system described by CPP includes two arrays, namely the PE array and the array memory, and the above description does not specify, either explicitly or implicitly, which one of the arrays is applicable in the description for

both the Array Interface and the Array Support Unit. Indeed, the Office Action's interpretation of Fig. 2.6 is unworkable because Fig. 2.6 shows the array interface only including signal lines for communicating addresses and 1-bit PE instructions. There is no data connection between the main memory and the PEs through the array interface and array support units because data cannot traverse through the array interface.

Claims 32, 40-41, 43-49 and 51 stand rejected under 35 U.S.C. 102(b) as being anticipated by Fung (U.S. Patent No. 4,380,046). This rejection is respectfully traversed.

Claim 22 recites, *inter alia,* "writing data from said plurality of processing elements to said memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements."

Claim 33 recites, *inter alia,* "wherein each of said data path circuits is further adapted to write data from said plurality of processing elements to said main memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements."

Claim 41 recites, *inter alia,* "wherein said circuit is further adapted to pass at least a portion of said data to said memory device in a vertical mode."

Claim 48 recites, *inter alia,* "wherein at least a portion of said data is stored in said memory device in a vertical mode."

Fung is directed to a massively parallel processor computer and discloses (e.g., at Fig. 1) a computer system including an array 22 of processing elements 44. The array 22 is also coupled to a CPU 29 via bus 29. Column 5, lines 4-10. Significantly, the computer system of Fung does not require conversion between vertical and horizontal modes of data storage. This is because the computer system of Fung lacks a main memory. More specifically, the processing element 44 of Fung (shown in greater detail in Fig. 2) includes a processing circuit (comprising counter/shifter 54, logic-slider sub-unit 56, and mask sub-

unit 58) which is coupled via a bidirectional single bit bus 52 to a local memory unit 50. The natural data format for each PE of Fung is therefore in the horizontal direction. As such, Fig. 2 shows no data conversion circuit interposed between the local memory unit 50 portion and the processing portion of the processing element. Indeed, since the data access performed by the general purpose CPU 26 is also in the horizontal direction, data is never needed or stored in the vertical direction in the computer system disclosed by Fung.

Claims 22, 33, 41, 48 each recite the use of a memory in a vertical direction. Fung therefore fails to teach or suggest the above recited limitations of independent claims 22, 33, 41, and 48. Accordingly, Fung also fails to teach or suggest the additional features claimed in claims 32, 40-41, 43-49 and 51.

Accordingly, independent claims 1, 11, 22, 33, 41, and 48 are believed to be allowable over the prior art of record. The depending claims (i.e., claims 2-6, 12-13, 24-27, 32, 35, 40, 43-44, 46-47, and 49-51) are believed to be allowable for at least the same reason as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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